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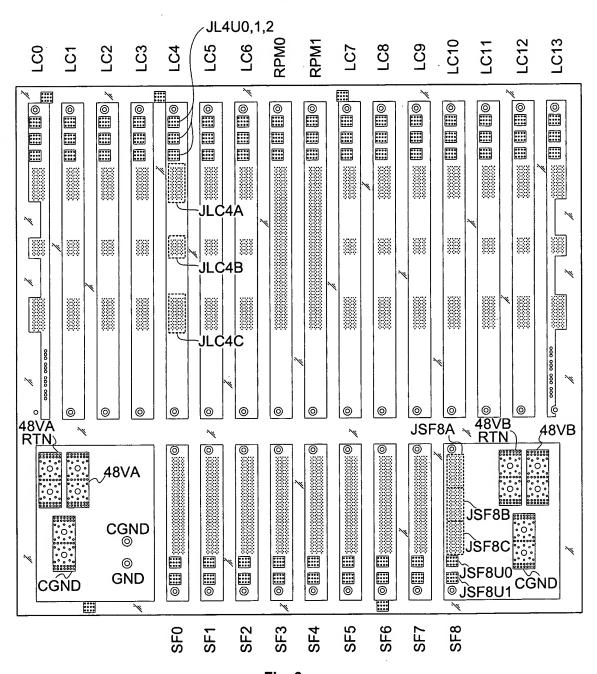


Fig. 3

<u>100</u>

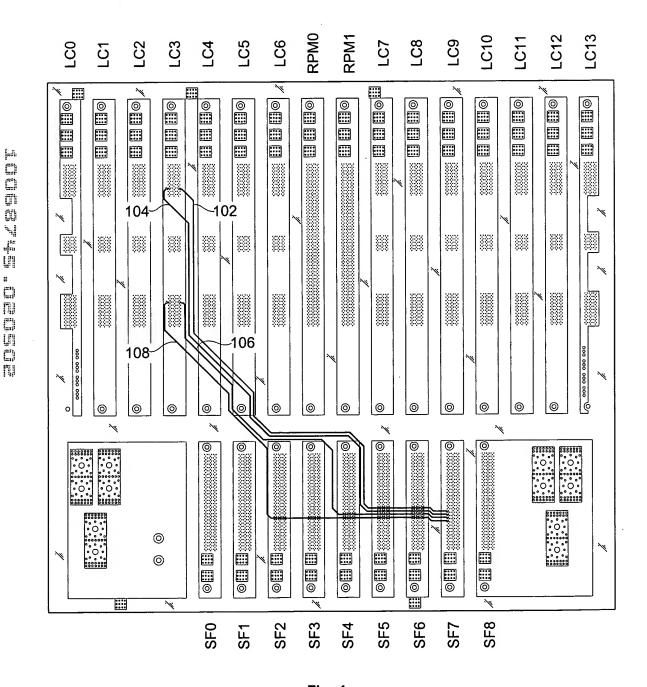
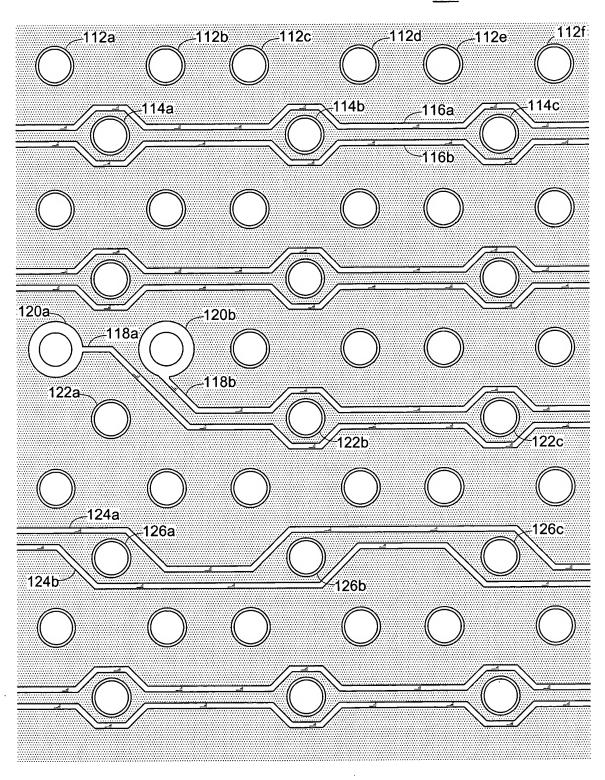


Fig. 4

<u>110</u>



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Fig. 5

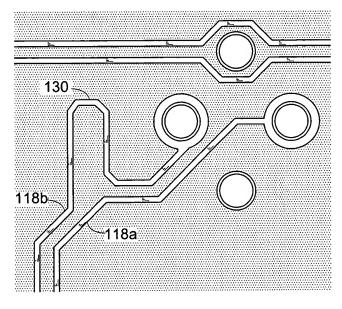


Fig. 6

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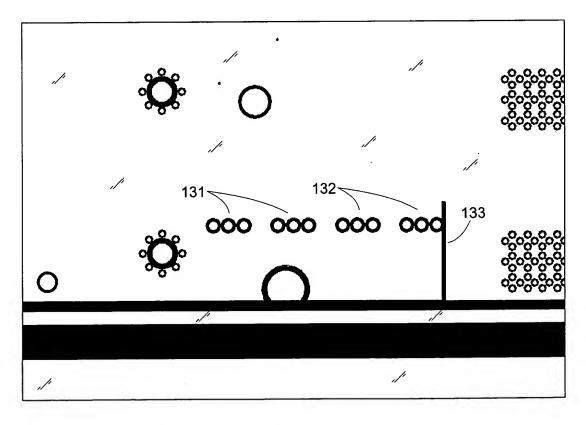


Fig. 7A

Inventor: Goergen

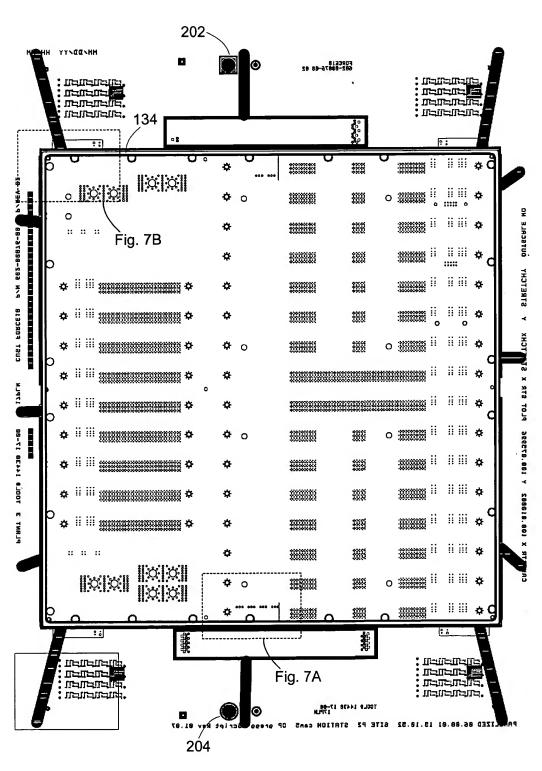
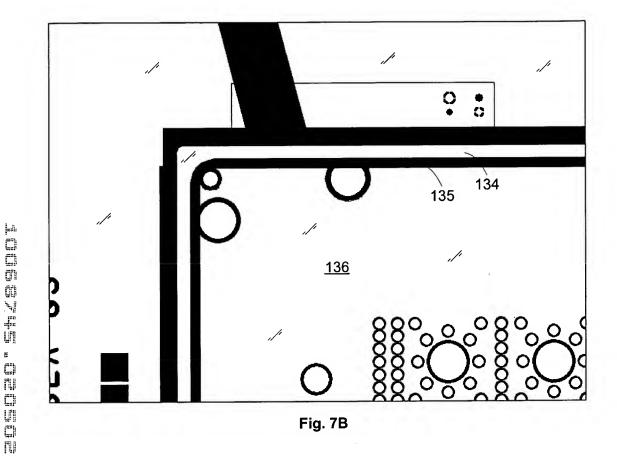


Fig. 7



<u>140</u>

Fig. 10

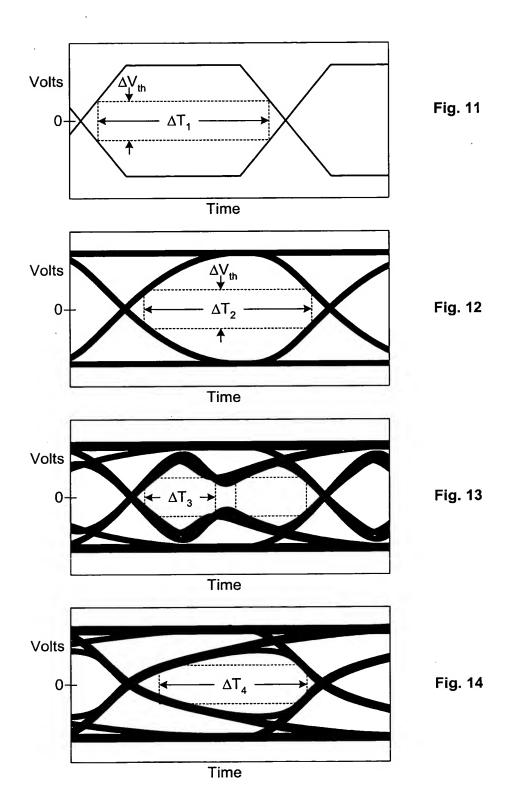
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Fig. 8

	Conductive Layers Layer No. Thickness Type			9/18	Insulating Layers Type Thickness	
		2.0	Foil/Plating	_		_
	L01{	1.2	Pads—		—Mask —B-stage	0.7 5.4
	L02	1.4	GND-		—Core	7.5
	L03	1.4	HS1—		—B-stage	6.5
	L04	1.4	GND-		—Core	7.5
	L05	1.4	HS2—		—B-stage	6.5
	L06	1.4	GND-		—Core	7.5
	L07	1.4	HS3—		—B-stage	6.5
	L08	1.4	GND-		—Core	7.5
	L09	1.4	HS4—		—B-stage	6.5
	L10	1.4	GND-		—Core	7.5
	L11	1.4	HS5—	<u></u>	—B-stage	6.5
	L12	1.4	GND		—Core	7.5
	L13	1.4	Signal x1 —		—B-stage	4.0
	L14	1.4	Signal y1 —		—Core	7.5
	L15	1.4	GND-	-	—Lam 2 B-stg	9.0
				-	—Lam 1 B-stg	8.5
	L16	5.6	A 48V rtn—	<u> </u>	—Core	6.0
	L17	5.6	A 48V dc			
	Fig. 9				—Lam 1 B-stg	
	9				—Lam 2 B-stg	
	L18	5.6	B 48V dc		—Lam 1 B-stg	8.5
				-	Core	6.0
	L19	5.6	B 48V rtn—	<u> </u>	—Lam 1 B-stg	8.5
					Lam 2 B-stg	
	L20	1.4	GND-		—Core	7.5
	L21 L22	1.4 1.4	Signal y2— Signal x2—		—B-stage	4.0
	L23	1.4	GND —		Core	7.5
	L24	1.4	HS6—		—B-stage	6.9
	L25	1.4	GND	-	—Core	7.5
	L26	1.4	HS7-		—B-stage	6.9
	L27	1.4	GND-	-	—Core	7.5
	L28	1.4	HS8		—B-stage	6.9
	L29	1.4	GND—	-	—Core	7.5
	L30	1.4	HS9—		—B-stage	6.9
	L31	1.4	GND—		—Core	7.5
	L32	1.4	HS10		B-stage	6.9
	L33	1.4	GND—		—Core	7.5
		1.4	Pads—		—B-stage	5.4
	L34{	2.0	Foil/Plating		Mask	0.7



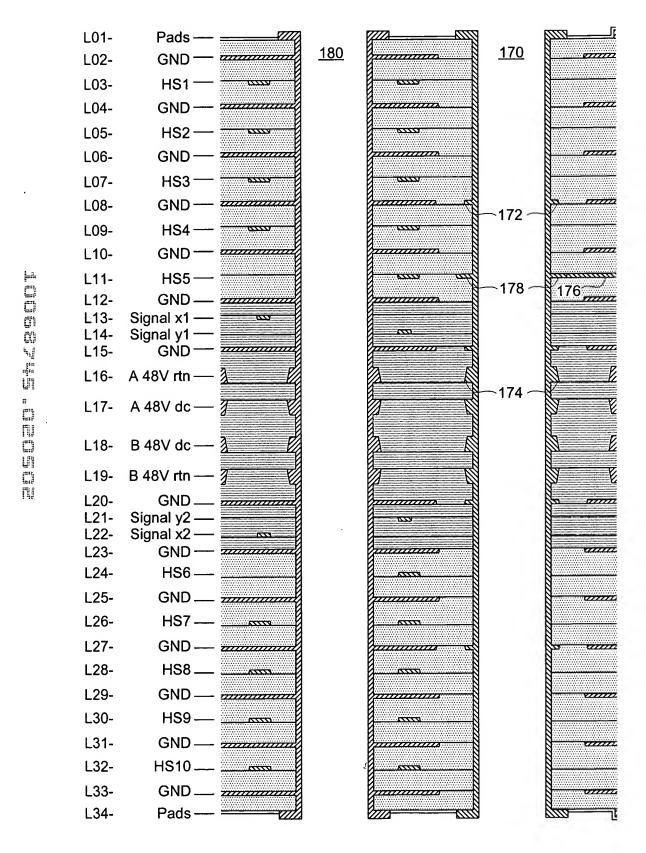
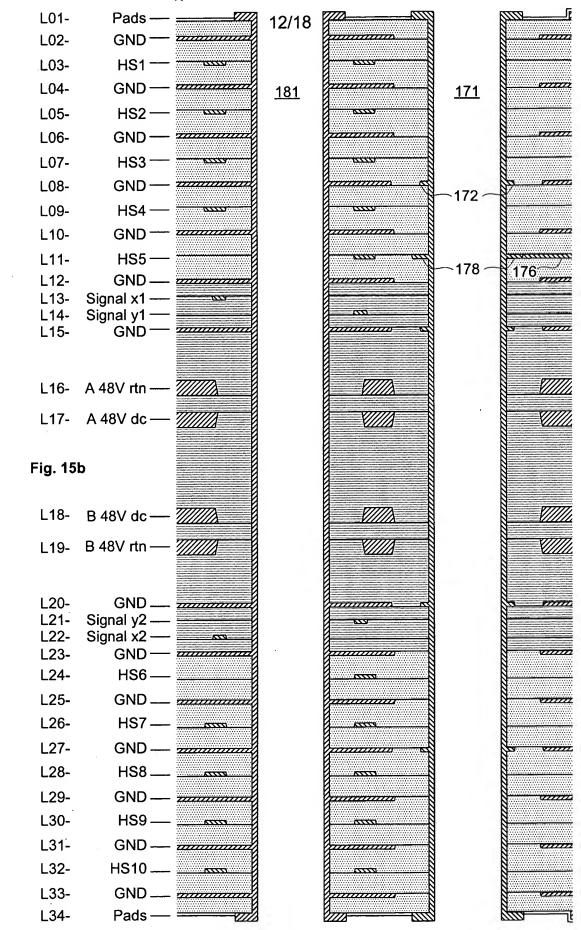
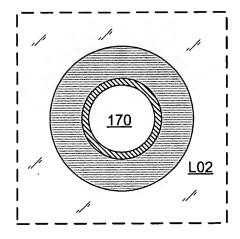


Fig. 15a



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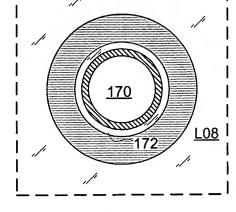


Fig. 16

Fig. 17

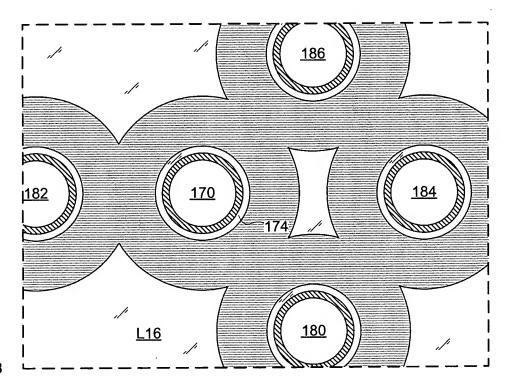
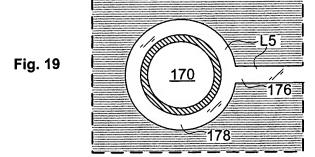
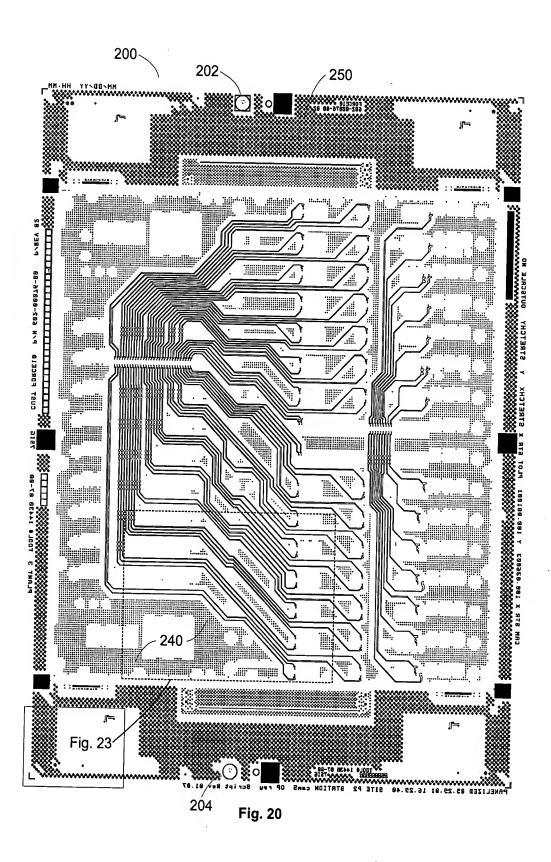
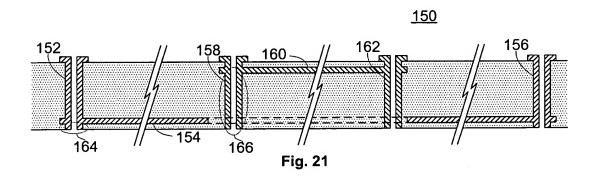
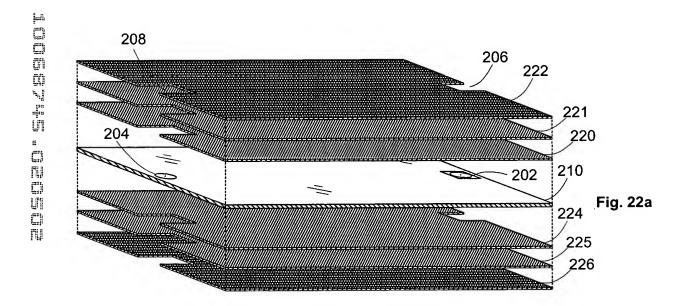


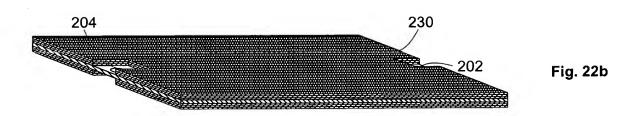
Fig. 18

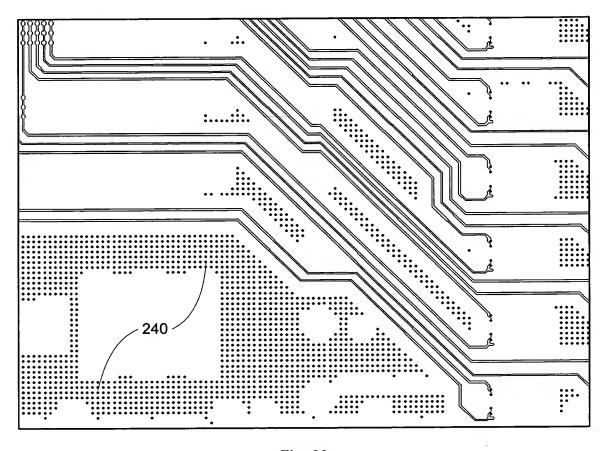








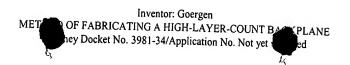




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Fig. 23



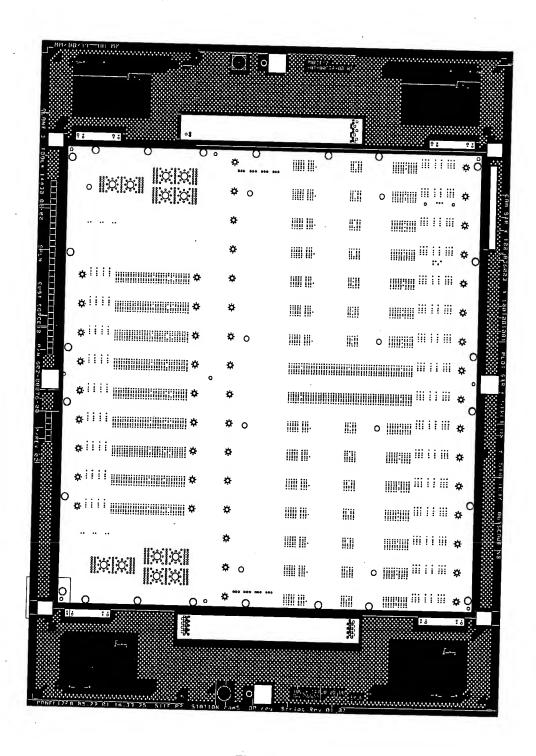


Fig. 24

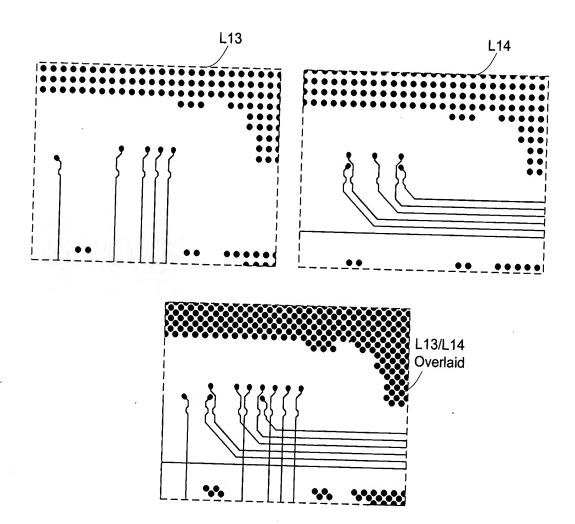


Fig. 25

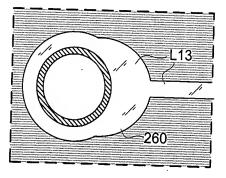


Fig. 26